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Xilinx Virtex-II FPGA based Processor PMC is First to have 64-bit Architecture for Easy Implementation of High Precision Arithmetic Digital Signal Processing

Oxford, UK, 29th April, 2003 – Orange Tree Technologies announces Zest100, a Processor PMC that releases the full performance potential of the Xilinx Virtex-II FPGA. 64-bit data paths from the FPGA to each memory bank and the PCI controller provide enormous bandwidth and easy manipulation of 64-bit precision data words.

The Virtex-II with 4 to 8 Million system logic gates provides vast processing power for applications such as radar, sonar, software radio, image processing, packet processing, and digital signal processing. With its 64-bit data paths Zest100 is particularly suited to high precision arithmetic but can also equally be used for low precision arithmetic with very high memory and I/O bandwidths. The PCI controller has been a particular focus to remove the classic I/O bottleneck, achieving a remarkable sustained bandwidth of 500MBytes/sec.. The 64-bit data paths to multiple double data rate (DDR) memory banks enable multiple 128-bit words to be accessed in every clock cycle. ASIC prototyping and development of intellectual property cores also benefit from this module's logic capacity and flexibility.

Charles Sweeney, Founder, commented "This is the platform that the Virtex-II has been waiting for, it allows the Virtex-II to deliver all its enormous potential. 64-bit architecture, high current power supplies, integrated cooling, and programmable clocks up to 500MHz provide the platform for any application to achieve its targets."

Block diagram and low resolution photograph are attached. Click here for high resolution photograph: http://www.orangetreetech.com/index_files/Zest100_highres.jpg

There are six memory banks, each with an independent 64-bit data path. Four banks connected to the FPGA are double data rate (DDR) SRAM with 4MBytes each. One further bank connected to the FPGA is 32 MBytes of DDR SDRAM. The remaining bank is 128 MBytes of SDRAM connected to the PCI controller and accessible from both the FPGA and the PCI bus. There is also 16MBytes of Flash.

The PCI controller has been specially selected as it not only achieves burst rates over 500MBytes/sec but sustained rates at that level as well.

Four programmable clocks generate frequencies from 400KHz to 500MHz. Their low jitter and high resolution provide great flexibility. They can be used on their own or with the Virtex-II on-chip Digital Clock Managers to enable applications to be run at their optimum frequency and with different clock domains.

The Processor PMC format provides extended height that caters for three 10 Amp power supplies, one of which is dedicated to the core logic of the FPGA. Cooling is integrated within the module and is provided on-board by a fan cooler or heatsink, again using

height allowed by the Processor PMC format. The card can plug into any PMC carrier card (for VME, cPCI, and PCI) and can form part of a complete system with other third party PMC modules.

I/O through the front panel is provided by a daughter card that plugs onto the Zest100. A variety of standard I/O functions is offered as well as a custom design service. Additional digital I/O is available via a header and the PMC I/O connector.

Full software support for Windows and VxWorks operating systems is provided, together with example logic cores for all the FPGA interfaces. These all help the user get their application up and running as quickly as possible.

Prices start at £4500 or \$7950 for the 4 Million gate version.

About Orange Tree Technologies

Founded in October 2001 by Charles Sweeney, previously a Co-founder of the EDA company Celoxica, Orange Tree Technologies is committed to providing the highest performance FPGA-based platforms. These modules plug into a variety of systems to deliver extreme data processing performance. Target markets include military, aerospace, telecommunications, imaging and machine vision, and industrial control. The website is www.orangetreetech.com

All trademarks are acknowledged.

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