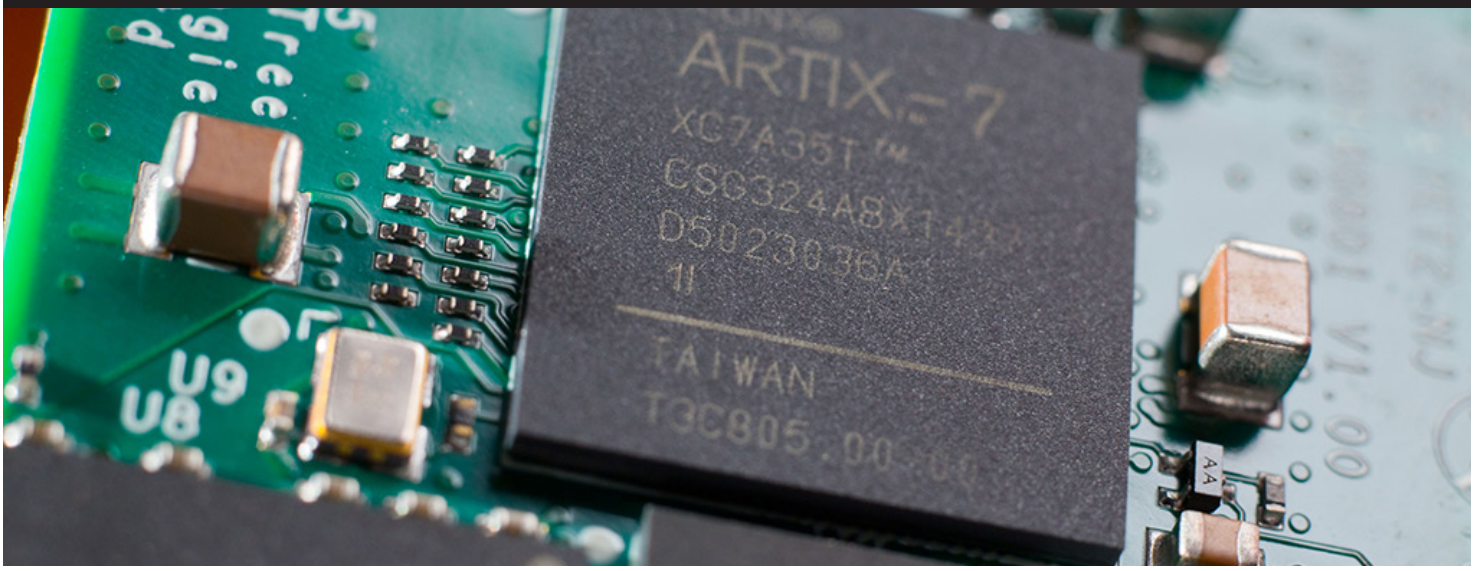
Orange Tree Technologies

ZestET2-NJ Datasheet



ZestET2-NJ: Gigabit Ethernet FPGA Module

Gigabit Ethernet FPGA module with hardware TCP/IP Offload Engine, which delivers a data rate of over 100MBytes/s in each direction, and a user programmable companion FPGA for connection to external devices.

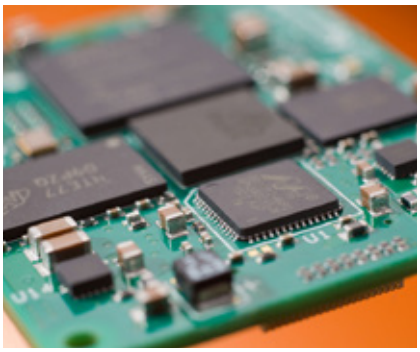
The ZestET2-NJ is an easy to use FPGA module with Xilinx Artix-7 user programmable FPGA and a very high performance TCP/IP Offload Engine (TOE) chip. It provides a simple bridge between a high speed computer network and a programmable digital interface. The TOE sustains a data rate over 100MBytes/s in each direction and includes a user programmable CPU for optional higher level protocols.

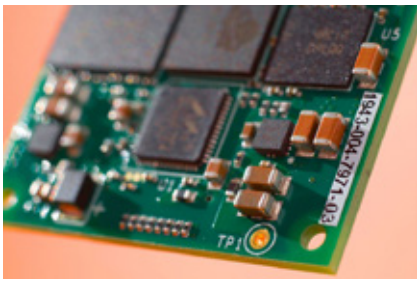
With its compact form factor (40mm x 50mm), the module is ideally suited to integration in embedded systems and OEM equipment. It features a user programmable Xilinx Artix-7 FPGA coupled with 512MBytes of high speed DDR3 memory. The FPGA can be programmed from on-board Flash, Ethernet or JTAG. It can be used as a programmable interface to external devices, for high speed processing of streaming data, and for data acquisition and control.

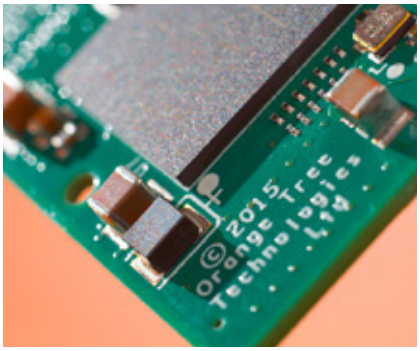
Fitted onto the ZestET2-NJ module is Orange Tree's third generation GigExpedite (GigEx) chip that delivers hardware UDP and TCP/IP Offload (TOE), 10/100/1000 Ethernet, an Ethernet MAC and embedded web server. This chip removes the network protocol processing burden from the user FPGA, which is particularly significant for Gigabit Ethernet.

GigEx has support for real-time applications in Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE). PTP synchronises devices on the network to a central time source device so that they can trigger operations at the same time and capture time-stamped events. SyncE enables each network device to generate a 125MHz clock synchronised across the network. These are protocols that run over Ethernet and therefore require no extra interconnect.

The third generation of Orange Tree's GigEx chip provides a user-programmable CPU completely free for the user to program for example with higher level Ethernet protocols such as GigE Vision and Industrial Ethernet, or it can be left unprogrammed. It has multiple and varied interfaces to the user FPGA including standard SPI and UART buses alongside a configurable high speed parallel interface. Full control of the GigEx device is possible via the low speed serial interfaces leaving the high speed parallel interface for data transfer.







Orange Tree Technologies Ltd
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Features:

- More than 100MBytes/s sustained data rate in each direction over Gigabit Ethernet
- Xilinx Artix-7 User FPGA and 512MBytes DDR3 memory
- Hardware TOE for UDP and TCP/IP offload
- User CPU within the TOE for application layer protocols
- Real-time Ethernet extensions Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE)
- Single power supply and low external component count

Benefits:

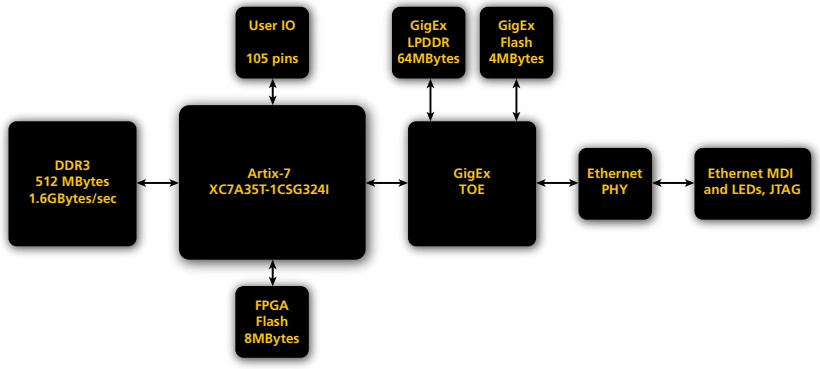
- Easy to use with no detailed networking knowledge required
- Devices connected to the User FPGA can communicate via Ethernet without using a processor or incurring processor overheads
- Virtually no FPGA resources used for talking to the network so most of FPGA available for data processing
- Can be extended to application layer protocols running above TCP or UDP either in User CPU or User FPGA

End Markets and Applications:

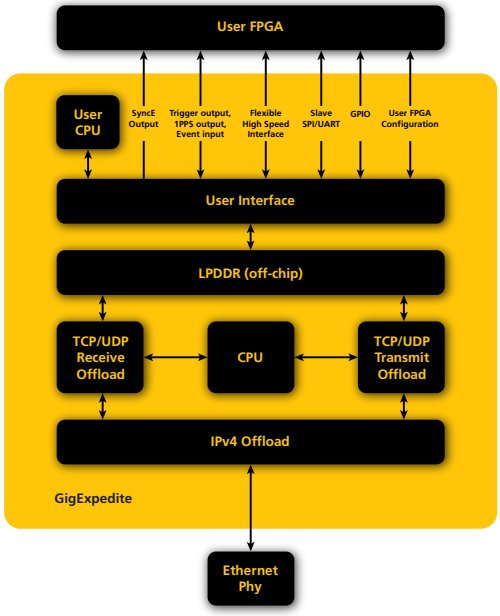
- Process Control
- Factory Automation
- Data acquisition
- Storage
- Remote Monitoring and Control Systems
- Machine Vision

Comparison of GigExpedite with traditional software stack running on an FPGA soft or hard core microprocessor

Feature	Software Stack	GigExpedite
Performance	Slower relative performance where the data rate depends on the processor power and load	Accelerated UDP and TCP/IP from dedicated hardware sustains over 100Mbytes/sec no matter what the system load
Power consumption	Higher power requirement due to need for fast processor	Low power hardware solution
Integration know-how needed for system design	Socket programming/ UDP and TCP/IP protocols/ Ethernet standards/ OS	Basic understanding of socket programming
Integration cost	High cost for software design integration and debugging	Low cost, rapid integration, flexible and varied interface options



ZestET2-NJ Block Diagram



ZestET2-NJ GigEx Block diagram

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Technical Specification	
Gigabit Ethernet	Marvell 88E1512 PHY transceiver and Orange Tree's GigEx TCP/IP Offload Engine with 64MBytes LPDDR SDRAM buffer (48MBytes buffering for network traffic).
GigEx Protocol Support	IPv4, TCP, UDP, DHCP Client, Auto IP, UPnP, HTTP, ARP, PTPv2.
GigEx User CPU	SPARC V8 32-bit processor 66MHz with 8MBytes LPDDR SDRAM and 256KBytes Flash. Standard GCC and Eclipse tools for code development and debugging over Ethernet are supplied with the board. This CPU can be programmed by the user for example with higher level Ethernet protocols, or it can be left unprogrammed.
Real-time Timing Support	PTPv2 protocol support allowing synchronisation of multiple modules across a network (requires external PTP master clock source). Timed trigger output, event capture and 1 Pulse Per Second generation. Synchronous Ethernet clock recovery and clock output signal.
GigEx Flash	256KBytes dedicated for user web pages.
GigEx – User FPGA Interfaces	High speed parallel interface to User FPGA for data transfer. SPI and UART interfaces for low speed data transfer.
User FPGA	Xilinx Artix-7 XC7A35T-1 Configurable from on-board User FPGA Flash, host computer via Ethernet, or JTAG
User FPGA Memory	512MBytes DDR3 400MHz 16 bits data bus, 1.6GBytes/sec bandwidth
I/O Connectors	Two Hirose DF12 connectors for 105 User FPGA IO signals One Hirose DF12 connector for MDI connections to Ethernet magnetics, User FPGA JTAG and power to the module.
User FPGA Flash	8MBytes for User FPGA configuration files and User FPGA application use
User FPGA Clock	50MHz oscillator for generating clocks within User FPGA
Power	Single 3.3V supply to the board. On-board high efficiency power supplies generate all other required voltages.
Physical	40 x 50 mm
Operating conditions	Industrial temperature range -40 to +85 deg C
Evaluation	A breakout board is available to simplify evaluation of the module. The breakout board has an RJ45 connector and connects the User FPGA IO pins to an FMC (FPGA Mezzanine Card) connector and a standard 0.1 inch connector for easy connection to external devices.
Host software	Windows and Linux software support for configuring and communicating with the User FPGA.
FPGA support	Logic cores for all FPGA interfaces. Supported by the Xilinx WebPack tools available for free download.
Examples	C, VHDL and Verilog source code for various examples.

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