Orange Tree Technologies

ZestET1: GigE TOE & FPGA Module

Features single-chip GigE hardware TCP/IP Offload Engine that delivers a data rate of over 100MBytes/s in each direction and a user programmable companion FPGA

The ZestET1 is a low cost, easy to use, very high performance GigE TCP/IP Offload Engine (TOE) and FPGA Module that provides a universal interface to quickly connect devices to a network at gigabit speed. It sustains a data rate of 100MBytes/s in each direction and can be used for existing and new product designs.

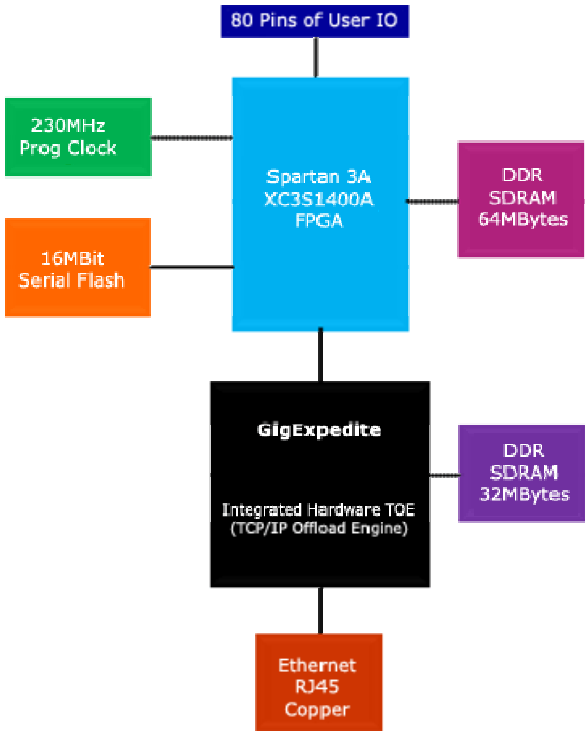
With its low price point, ease of use and compact form factor (50mm x 75mm), the module is ideally suited to integration in embedded systems and OEM equipment. It features a user programmable Xilinx Spartan-3A FPGA with up to 1.4M system gates that are completely free for user programming. The FPGA can be programmed from on-board Flash, Ethernet or JTAG and is capable of running soft-core processors and higher level protocols such as GigE Vision and Industrial Ethernet. It can also be used as a programmable interface to external devices, for processing data on the fly, high speed processing of streaming data and controlling external devices.

Fitted onto the ZestET1 module is Orange Tree's GigExpedite (GigEx) chip that delivers hardware UDP and TCP/IP Offload (TOE), Tri-Speed Ethernet, an Ethernet MAC and embedded web server. The ET1's GigEx device supports IPv4, UDP and TCP transport layer protocols with higher level protocols and applications supported using the companion FPGA.

The GigEx integrated hardware TCP/IP stack including hardware UDP and TCP/IP Offload Engine (TOE) removes the network protocol processing burden from the companion FPGA or embedded processor.

Resource-intensive memory copies, checksum computation and reassembling of out-of-order packets are handled by the GigEx hardware TOE. This allows a smaller, lower cost CPU to be deployed in the system; or potentially a soft-core within the companion FPGA, with its resources being allocated to running applications, rather than handling network traffic.

ZestET1 GigE TOE & FPGA Module



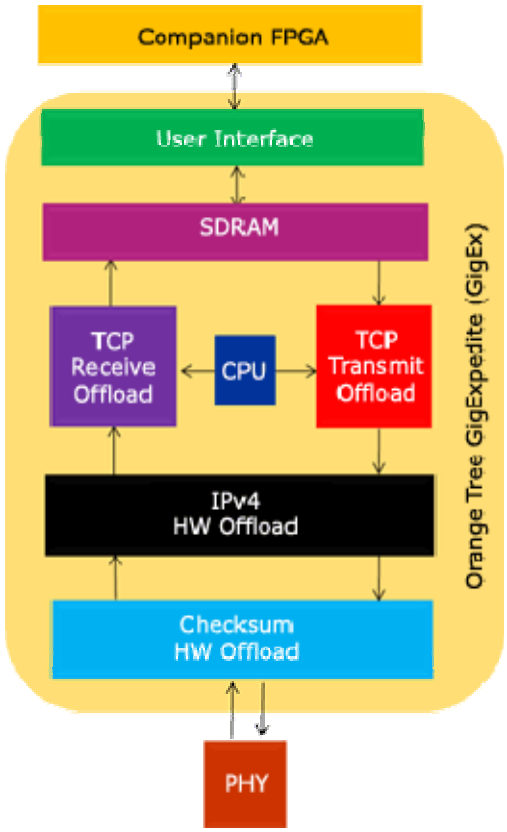
ZestET1 GigE TOE & FPGA Module

The board-level embedded hardware and software solutions Company

ZestET1 GigExpedite Integrated Hardware UDP and TCP/IP Offload Engine (TOE)

Feature	Software Stack	ZestET1 GigExpedite™
Performance	Slower relative performance	Accelerated UDP and TCP/IP from dedicated hardware
Power Consumption	Higher power requirement due to need for fast processor	Low power hardware solution
Modular System BOM Cost	Higher system cost through larger CPU and memory requirements	Low cost. No uP needed or a soft core uP in the companion FPGA can be used for processor functions
Integration Cost	High cost for software design integration and debugging	Low cost, rapid integration
Integration Know-how Needed for System Design	Socket programming/ UDP and TCP/IP protocols/ Ethernet standards/ OS	Socket programming

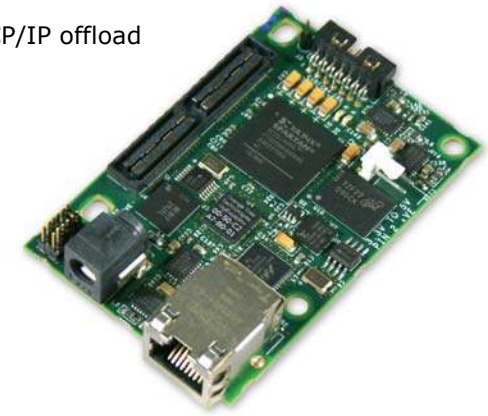
ZestET1 GigExpedite Integrated Hardware UDP and TCP/IP Offload Engine (TOE) Block Diagram



The GigEx integrated hardware TCP/IP stack including hardware UDP and TCP/IP Offload Engine (TOE) removes the network protocol processing burden from the companion FPGA or embedded processor. Designed for programming ease-of-use it provides a very high performance, robust and cost-effective real-time Ethernet solution that is interoperable with standard Ethernet infrastructure.

Benefits:
Low Cost and easy to use with no detailed networking knowledge required
Offers simple access to very fast data rates over Ethernet without having to integrate complex networking hardware and software
Devices can communicate via Ethernet without using a processor or incurring processor overheads
Can be quickly and cost-effectively extended to application layer protocols

Features:
More than 100MBytes/s sustained data rate in each direction
User programmable companion FPGA supports low cost, soft core processor implementation and application layer protocols
High reliability and high stability hardware TOE for UDP and TCP/IP offload



End Markets and Applications:
Process Control
Factory Automation
DAQ
Storage
Remote Monitoring and Control Systems
Machine Vision

Technical Specification

Gigabit Ethernet	Marvell 88E1118R PHY transceiver and Orange Tree's GigEx TCP/IP Offload Engine with 32MBytes DDR SDRAM buffer.
GigExpedite Protocol Support	IPv4, TCP, UDP, DHCP Client, Auto IP, UPnP, HTTP, ARP.
FPGA	Xilinx Spartan-3A XC3S1400A in FTG256 package. FPGA configuration: On-board Flash at power up, or Ethernet, or JTAG.
FPGA Memory	64MBytes DDR SDRAM, DDR333 speed, 16 bits data bus.
I/O Connector	High density impedance controlled Samtec QSH 120 pins - 80 FPGA IO pins of which 76 may be differential pairs and the other 4 are inputs; FPGA JTAG; board input power; FPGA IO power. Cable or board may be plugged into the connector. Breakout board for 0.1" headers available. IO Voltage set by jumpers to 3.3V, 2.5V, 1.8V, 1.2V or voltage supplied from IO connector. Integrated differential termination resistors in the FPGA.
Flash	16Mbit serial SPI Flash for FPGA configuration and general storage.
Clock	Programmable clock chip up to 230MHz, programmable over Ethernet and retains settings after power cycling. FPGA can synthesize higher clock speeds internally.
Power	Single 3.3V or 5V input to the board from 2.5mm power jack, or 2-pin latched header, or the IO connector. On-board high efficiency power supplies generate required voltages.
Companion FPGA Design Software	Free Xilinx design tool ISE WebPACK available from http://www.xilinx.com/ise/logic_design_prod/webpack.htm
Logic cores	Interface to the GigEx TOE, DDR SDRAM controller.
Examples	C, VHDL and Verilog source code for various examples.
Physical	75 x 50 mm

The board-level embedded hardware and software solutions Company

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