



# Zest100 FPGA PMC

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Zest100 is a very high performance processing engine that uses a Xilinx® Virtex-II® FPGA as the processing component. These FPGA's are used increasingly in compute-intensive applications such as networking, radar, imaging and telecoms, and also for prototyping ASIC's and developing IP cores.

This is a PMC, an industry-standard module, which has been designed to achieve the maximum possible performance from the Virtex-II. The largest Virtex-II can be accommodated and it is accompanied by a PCI controller and memory devices selected for their very high sustained I/O bandwidths. Support software and IP cores for the interfaces make this module very easy to use.

#### Main benefits:

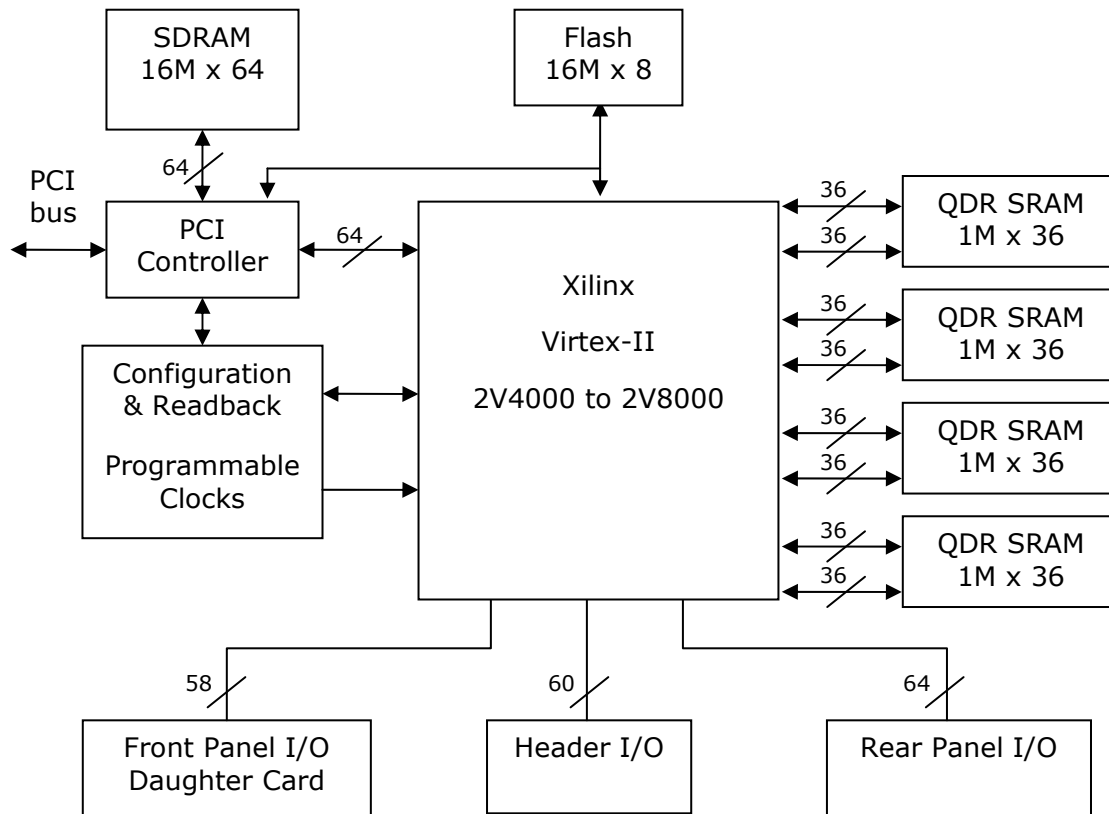
- Modular for building complete systems comprising one or more cards and PMC modules from third parties. Four I/O ports enable connection to external systems or other cards in the same system.
- Virtex-II FPGA's are extremely well suited to digital signal processing operations. Devices from 2V4000 to 2V8000 (the largest Virtex-II) provide scope to choose an FPGA large enough for all the user's potential applications, so avoiding unnecessary partitioning across multiple FPGA's.
- 64-bit precision arithmetic is supported by the 64-bit data width of all the memory interfaces and the PCI controller, while 32, 16, and 8 bit word widths are also supported. This provides the highest possible memory bandwidth for all data widths. Within the FPGA any word width may be used.
- Communication with other cards on the PCI bus at the full sustained data rate (not just peak burst rate) of the PCI bus is achieved through the use of a PCI controller that achieves ~500MBytes/sec sustained (many PCI controllers do not achieve even half this sustained rate).

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- Large data sets can be stored locally in a bulk memory bank. It is 128 Mbytes of Synchronous DRAM and is accessible from both the PCI bus and the FPGA via the PCI controller so requires no controller logic within the FPGA.
- Scratchpad memory for intermediate data processing storage at extremely high bandwidth is provided by four QDR (Quad Data Rate) SRAM memory banks of 4 Mbytes each, 16 Mbytes in total. Each bank has a completely independent interface to the FPGA to enable parallel processing. QDR transfers two words per clock cycle in each direction on two separate write and read data buses. The data bus widths are 36 bits in each direction and simultaneous writes and reads can be performed. With two words per clock cycle in each direction this gives an effective 72 bits data bus width for both writes and reads in every clock cycle.
- Non-volatile application data and FPGA configuration files can be stored in 16Mbytes of Flash. The configuration files enable the FPGA to configure on power-up.
- Multiple clock domains within the FPGA can be driven by four programmable clocks that are external to the FPGA. They can generate up to 500MHz with very low jitter, as required by synchronous memory and other devices, and have fine resolution for specifying the clock frequency. The Virtex-II on-chip Digital Clock Managers can also be used to create further on-chip clocks.
- The FPGA can operate at the highest possible clock rates as on-board high current power supplies and on-board fan cooling are provided.
- Any PMC carrier board can be used as fan cooling is provided on-board rather than relying on a fan embedded in the carrier board.
- Multiple I/O options and Front Panel I/O daughter cards provide flexibility for interfacing to external devices.
- Debugging is supported by FPGA configuration and readback over the PCI bus or JTAG header.
- Wide range of target systems supported by carrier boards in PCI, cPCI and VME formats; and support software for Windows 2000 and XP, Linux, and VxWorks.
- Example memory interface cores are supplied with the board, and many application logic cores are available from Xilinx and other third parties.
- Board support packages enable high level application development with popular DSP and system level design tools.
- Full application libraries will be offered in due course and will enable the board to be used without any programming by the user.

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## Specification

**FPGA.** The Xilinx Virtex-II from 2V4000 to 2V8000 is available in all speed grades.

### Memory.

- 128MBytes of 100MHz SDRAM is controlled by the PCI controller and is accessible from both the PCI bus and the FPGA. An arbiter within the PCI Controller controls which device has access.
- Four banks of 4MBytes each QDR SRAM are connected to the FPGA.
- 16MBytes of Flash is available for configuration and user-defined purposes.

All memory banks have 64-bit data paths per clock cycle (Flash is 8 bits and the SRAM also have 1 parity bit per 8 data bits).

The QDR memory clocks are source-synchronous to achieve maximum data rates. Source synchronous means that in both reading and writing, the data clock is driven with the data from the source of the data to the receiver. The QDR devices can also be used as single data rate devices, if required, by reading only one of the two words per cycle and by writing only one of the two words per cycle.

**PCI Controller.** This has been selected for the highest sustained PCI bandwidth, achieving up to 528MBytes/sec both peak and sustained. It has four independent DMA controllers with a total of 2KBytes buffer. The PCI bus is 64 or 32-bit, 66 or 33 MHz, and 3.3V or 5V PCI signaling.

**Clocks.** Two programmable clocks generate up to 500MHz and two others generate up to 120MHz, all with very low skew and jitter as required by synchronous memory devices. They are programmable from the PCI bus and have resolutions of about 0.01MHz to 1MHz, increasing as the output frequency increases. Further clocks can be generated within the FPGA using the Virtex-II's twelve Digital Clock Managers.

**Configuration.** The FPGA is configured using the high speed SelectMap port from either the PCI bus or the Flash, or from JTAG header. It can also be readback over PCI or JTAG for debugging.

**I/O.** There are four I/O ports as described below.

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- PCI via PCI Controller - 64/32 bits, 66/33 MHz, 5V or 3V3 signaling
- PMC user defined I/O - 64 signals connected between the FPGA and the PMC user defined I/O connector
- Header - 60-pin straight header with all pins connected to the FPGA
- Front Panel - one of a range of I/O daughter cards plugs onto a 60-pin straight header with 58 pins connected to the FPGA and 2 pins for 5V and 3V3 power. A connector on the daughter card is accessible through the card's front bezel. I/O daughter cards have different front bezel connectors for connection to different systems.

Note that 9 of the FPGA signals connected to the Header and the Front Panel header are shared.

**Power.** Both 5V and 3V3 power from the carrier card are used. Up to about 18W is required from the 5V power, of which up to 15W is available for the Virtex-II core as 10A @ 1.5V. The actual figure depends on the current drawn by the FPGA when running the user's application. For a spreadsheet power consumption estimator see [http://www.xilinx.com/support/techsup/powerest/virtex2\\_power\\_estimator\\_v105.xls](http://www.xilinx.com/support/techsup/powerest/virtex2_power_estimator_v105.xls).

The other devices and Virtex-II I/O power are derived from the 3V3 power supply. The estimated maximum power consumption of these devices is 10W, but again the actual figure depends on the application.

**Cooling.** The FPGA core and I/O may dissipate up to about 20W. With an ambient temperature of 40 deg C and a maximum chip junction temperature of 80 deg C, the maximum thermal resistance from junction to air is  $(80 - 40)/20 = 2.0$  deg C/W. This can only be achieved either by a heatsink with forced air cooling or by a fan cooler. Allowance has been made on the PCB for mounting a heatsink or fan cooler rather than gluing direct to the FPGA, which can stress the FPGA solder joints. Heatsink or fan cooler is supplied. The other chips and DC/DC converters can be convection cooled in still air. Operating ambient temperature range is 0-40 deg C.

**Monitors.** Ambient temperature and all power supply voltages are monitored.

**Physical.** The card format is Single-sized Processor PMC or PrPMC for short. This is a development of the PMC (PCI Mezzanine Card) standard and is intended for PMC's that have processors on them and therefore require higher power consumption and cooling than I/O PMC cards. The maximum allowed power is determined by the connectors' rated current rather than being limited to 7.5W on PMC. Also extra height is allowed for heatsinks or fan coolers on Side 2, the side facing away from the carrier card. Since Virtex-II FPGA's can use 20W or even more, the PrPMC format is necessary for adequate power supply and cooling.

- Conforms to Processor PMC Standard, VITA 32—2003. The card is a Non-Monarch (i.e. slave) so does not perform PCI configuration of the other devices on the PCI bus following reset.
- Plugs into standard PMC carrier card Single-size PMC slot.
- Maximum height of the module above the carrier board is from 26.0 to 33.5mm. The actual height depends on the heatsink/fan cooler option selected.
- 5V and 3V3 power are required.
- 5V or 3V3 signaling on the PCI bus i.e. 'universal'.

As with any card, the height, power consumption and cooling method should be checked for compatibility with the target system.

Great care has been taken in all aspects of the design to ensure reliability. The Processor PMC format has been followed to allow space for the use of high current power supplies and a substantial heatsink or fan cooler mounted on the module. The power distribution system includes a range of decoupler values for low power supply impedance over a broad range of operating frequencies. PCB tracks are impedance controlled, and series or parallel terminations are used where appropriate, for example on all clock signals.

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Disclaimer—This information is subject to change without notice. Some features are not available in all variants of the product. All clock rates quoted are taken from the datasheets of the respective components, and achievable clock rates will depend on the speed grade of the FPGA and on the design running in the FPGA.